Notice of Allowability	Application No.	Applicant(s)	
	10/616,958	SLAVIN, KEITH R.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/19/07*.

2. ☒ The allowed claim(s) is/are *1-56*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

Examiner's statement for reason for allowance

1. Claims **1-56** have been allowed.

As per claim 1:

The prior art of record, Ichiriu (U.S. PN: 7,002,823) in figure 1 disclose a CAM device (100) includes a CAM array (101) (the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words), error detector (107), priority encoder (114), comprand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) (145), address bus (ABUS) (141) and comparand bus (CBUS) (143). The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Further, the CAM array (101) is coupled to comprand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101) (see col. 3, lines 29-6.

The prior art of record, Hata et al. (U.S. PN: 6,842,359) in FIG. 1 disclose a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match

detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58) (see col. 6, lines 22-33).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious an encoding circuit for encoding an incoming CAM word to produce an encoded CAM word such that a one-bit mismatch between a comparand and said incoming CAM word results in at least a M-bit mismatch between said encoded CAM word and a similarly encoded comparand, a circuit for precharging a match line to a predetermined state before a comparison between said encoded CAM word and said similarly encoded comparand and a memory storage location for storing said encoded CAM word. Consequently, claim 1 is allowed over the prior art.

Claims **2-13,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 14:

The prior art of record, Ichiriu (U.S. PN: 7,002,823) in figure 1 disclose a CAM device (100) includes a CAM array (101) (the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words), error detector (107), priority encoder (114), comprand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) (145), address bus (ABUS) (141) and comparand bus (CBUS) (143). The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Further, the

CAM array (101) is coupled to comprand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101) (see col. 3, lines 29-6.

The prior art of record, Hata et al. (U.S. PN: 6,842,359) in FIG. 1 disclose a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58) (see col. 6, lines 22-33).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a masking device for producing a masked TCAM word by masking off all bits in an incoming TCAM word that are not used in a matching prefix, an encoding circuit for encoding said masked TCAM word to produce an encoded TCAM word such that a one-bit mismatch between a comparand and said incoming TCAM word results in at least a M-bit mismatch between said encoded TCAM word and a similarly encoded comparand, a circuit for precharging a match line to a predetermined state before a comparison between said encoded TCAM word and said similarly encoded comparand and a memory storage location for storing said encoded TCAM word. Consequently, claim 14 is allowed over the prior art.

Claims **15-28,** which is/are directly or indirectly dependent/s of claim 14 are also allowable over the prior art of record.

As per claim 29:

The prior art of record, Ichiriu (U.S. PN: 7,002,823) in figure 1 disclose a CAM device (100) includes a CAM array (101) (the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words), error detector (107), priority encoder (114), comprand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) (145), address bus (ABUS) (141) and comparand bus (CBUS) (143). The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Further, the CAM array (101) is coupled to comprand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101) (see col. 3, lines 29-6.

The prior art of record, Hata et al. (U.S. PN: 6,842,359) in FIG. 1 disclose a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58) (see col. 6, lines 22-33).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious an encoding circuit for encoding an incoming CAM word to

produce an encoded CAM word such that a one-bit mismatch between a comparand and said incoming CAM word results in at least a M-bit mismatch between said encoded CAM word and a similarly encoded comparand, a circuit for precharging a match line to a predetermined state before a comparison between said encoded CAM word and said similarly encoded comparand and a memory storage location for storing said encoded CAM word. Consequently, claim 29 is allowed over the prior art.

As per claim 30:

The prior art of record, Ichiriu (U.S. PN: 7,002,823) in figure 1 disclose a CAM device (100) includes a CAM array (101) (the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words), error detector (107), priority encoder (114), comparand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) (145), address bus (ABUS) (141) and comparand bus (CBUS) (143). The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Further, the CAM array (101) is coupled to comparand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101) (see col. 3, lines 29-6.

The prior art of record, Hata et al. (U.S. PN: 6,842,359) in FIG. 1 disclose a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58) (see col. 6, lines 22-33).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a masking device for producing a masked TCAM word by masking off all bits in an incoming TCAM word that are not used in a matching prefix, an encoding circuit for encoding said masked TCAM word to produce an encoded TCAM word such that a one-bit mismatch between a comparand and said incoming TCAM word results in at least a M-bit mismatch between said encoded TCAM word and a similarly encoded comparand, a circuit for precharging a match line to a predetermined state before a comparison between said encoded TCAM word and said similarly encoded comparand and a memory storage location for storing said encoded TCAM word. Consequently, claim 30 is allowed over the prior art.

Claims **31-42,** which is/are directly or indirectly dependent/s of claim 30 are also allowable over the prior art of record.

As per claim 43:

The prior art of record, Ichiriu (U.S. PN: 7,002,823) in figure 1 disclose a CAM device (100) includes a CAM array (101) (the CAM array includes a plurality of CAM cells arranged in rows for storing CAM words), error detector (107), priority encoder (114), comparand register (115) and read/write circuit (161). Instructions, addresses and commands are input to the CAM device via an instruction bus (IBUS) (145),

address bus (ABUS) (141) and comparand bus (CBUS) (143). The CAM array also includes a validity storage (102) to store validity values and each validity value corresponds to a respective row of CAM cells and indicates whether the row contains a valid CAM word (each validity value may be represented by a single bit or multiple bits). Further, the CAM array (101) is coupled to comprand register (115) which also the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and during a compare operation, the comparand masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array (101) (see col. 3, lines 29-6.

The prior art of record, Hata et al. (U.S. PN: 6,842,359) in FIG. 1 disclose a CAM device (10) includes a CAM cell array (12), a search-bit line driver (14), a match detection circuit having a match line pre-charge circuit (16) and a match line sense circuit (18) (see col. 5, lines 51-58) (see col. 6, lines 22-33).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious encoding masked TCAM word to produce an encoded TCAM word such that a one-bit mismatch between a comparand and said incoming TCAM word results in at least a two-bit mismatch between said encoded TCAM word and a similarly encoded comparand, precharging a match line to a predetermined state before a comparison between said encoded TCAM word and said encoded comparand and storing said encoded TCAM in a memory storage location of said TCAM device. Consequently, claim 43 is allowed over the prior art.

Claims **44-56,** which is/are directly or indirectly dependent/s of claim 43 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned (571) 273-8300.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100